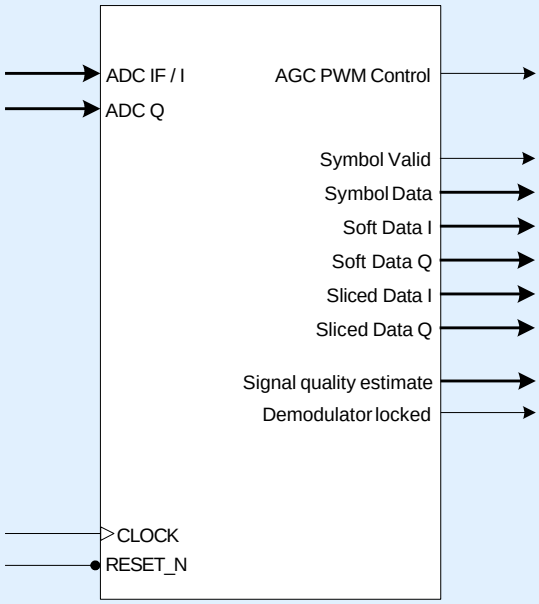
Universal QAM Demodulator

CMS0006

- IF sub-sampling or I/Q baseband interface.
- Variable ADC width support.
- Single external clock source required.
- Single external analogue loop for AGC.
- Fully digital and automatic timing & frequency recovery - no VCXO or AFC required.
- Fully-digital matched channel filter for robust performance in the presence of ACI.
- Blind and decision-directed adaption algorithms ensure rapid convergence of AGC, PLL and equaliser sub-systems.
- Automatic channel equalisation using LTE and DFE algorithms - signal quality estimate available.
- Symbol rate recovery up to approximately 40% of the master clock frequency.
- Large QAM support: BPSK, (O)QPSK, 8, 16, 32, 64, 128, 256
- Number of synthesis options to optimise speed (& therefore symbol rate) vs. area.
- Software programmable symbol demapping.
- Implementation loss of <1dB for 128 or 256-QAM, and <0.5dB for other supported QAM modes.
- Integrates with Commsonics CMS0004(QAM Modulator) , CMS0003(FEC) and CMS0002(Viterbi) cores to form a complete broadband PHY.
- Number of debug signals available - carrier, timing lock, frequency offset etc.



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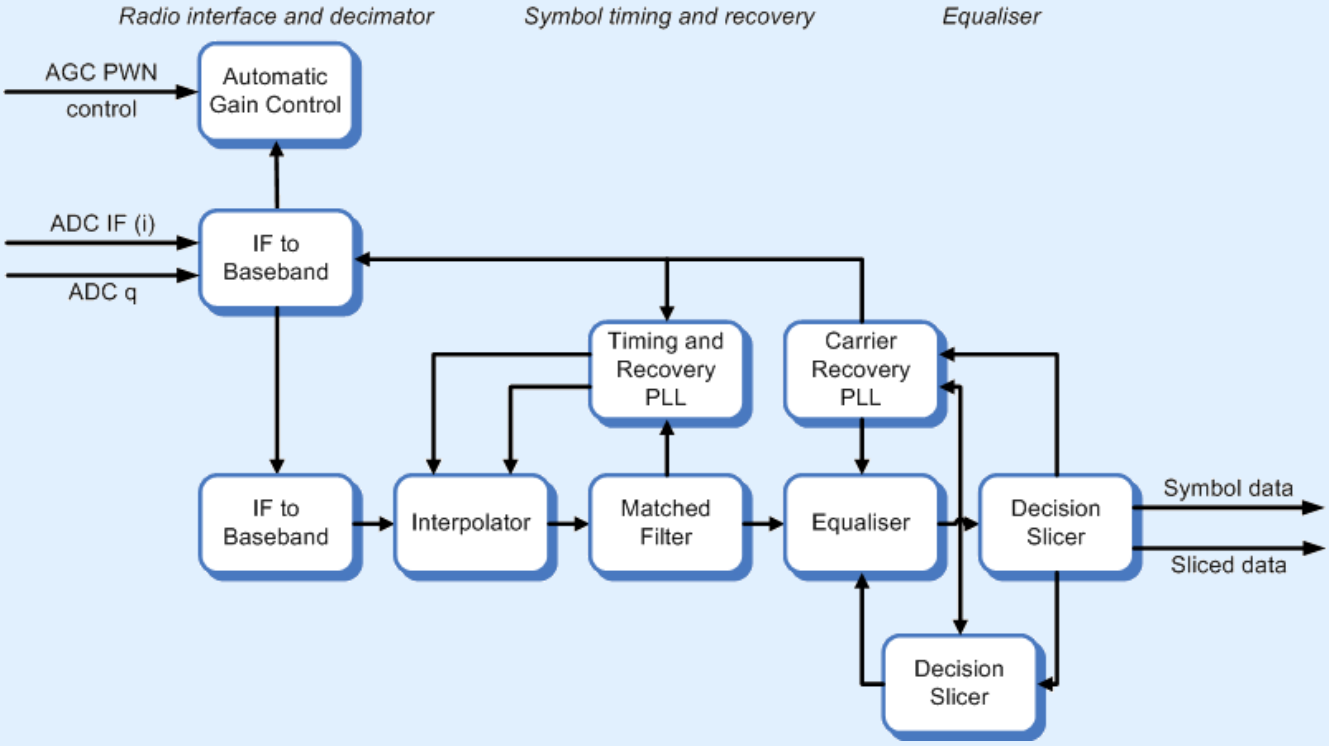
Block Diagram

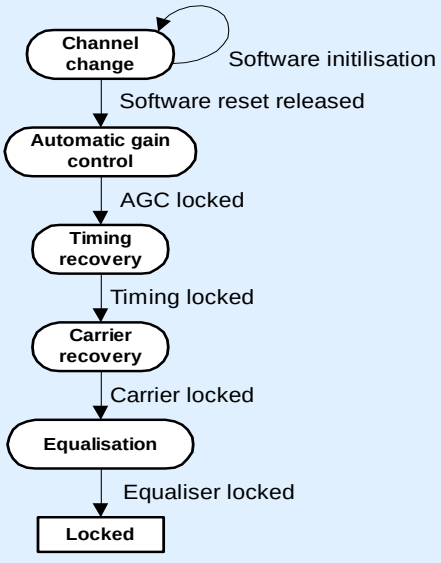


Detailed Description

The Commsonic CMS0006 Universal QAM Demodulator is a 4th generation design that exploits Commsonic's experience of QAM and OFDM systems for broadband terrestrial, satellite and cable modems.

The demodulator core has been designed to lock robustly in the presence of noise, frequency & timing offsets, static & dynamic multi-path channels and various other forms of interference. The demodulator core consists of three major sub-modules: the Radio interface & decimator, Symbol timing recovery and the Equaliser.

The operation of the demodulator is fully automated by an internal state machine.



Detailed Description (Cont'd)

A description of the processing steps follows:

Radio interface and decimator

The radio interface and decimator (RID) module is responsible for generating down-converted and filtered samples of the QAM input signal by performing external (analogue) gain control; IF mixing and image & decimation filtering.

ADC IF / I. The I component (or IF sub-sample) of the QAM input signal sampled at the input CLOCK rate. The format is configurable between 2's complement and offset binary.

ADC Q. The Q component of the QAM input signal sampled at the input CLOCK rate. The format is configurable between 2's complement and offset binary. Not used when IF sub-sampling is used.

AGC PWM control. A PWM control signal output to increase/decrease the gain of an external VGA. This allows the radio interface to control the level of the signal at the ADC input(s) to minimise the distortion due to clipping or quantisation.

Symbol timing recovery

The symbol timing recovery (STR) module is responsible for generating correctly timing constellation samples of the baseband & filtered signal by performing channel filtering; symbol rate detection and timing recovery.

Equaliser

The equaliser (EQU) module is responsible for generating the original QAM constellation by performing carrier frequency recovery; channel acquisition, equalisation & tracking and DC offset correction. The demodulator provides 3 types of outputs:

Soft data I & Q. The demodulated QAM constellation devoid of timing and frequency offsets and with any multi-path interference removed. These outputs provide a diagnostic indication of the success of the demodulation. Alternatively, an external slicer and de-mapper can use these outputs to recover the bit stream.

Sliced data I & Q. The internally sliced *soft data I &Q* signals. An external symbol de-mapper can use these outputs to recover the bit stream.

Symbol data. The internally de-mapped constellation symbol. The de-mapping table can be fixed at synthesis or software programmable.

In addition the EQU provides a signal quality estimate calculated from the demodulated constellation noise. The estimate is available either from a software register or as signal output.

Synthesis Parameters

The CMS0006 core provides a number of synthesis options to allow the core to be optimised for its target application; for example, the length and structure of the equaliser can be tailored to suit the propagation conditions and may be omitted entirely where dispersion is not an issue.

The CMS0006 core may be optimised for either ASIC or FPGA synthesis to maximise the utilisation of the target architecture.

Register Configuration

The CMS0006 core is designed to acquire and lock to the input signal automatically with the external software application only specifying the input QAM order. A number of expert registers are provided to allow the various control loop bandwidths and gains to be tweaked to ensure successfully demodulation even in the severest of environments.

Principle I/O Description

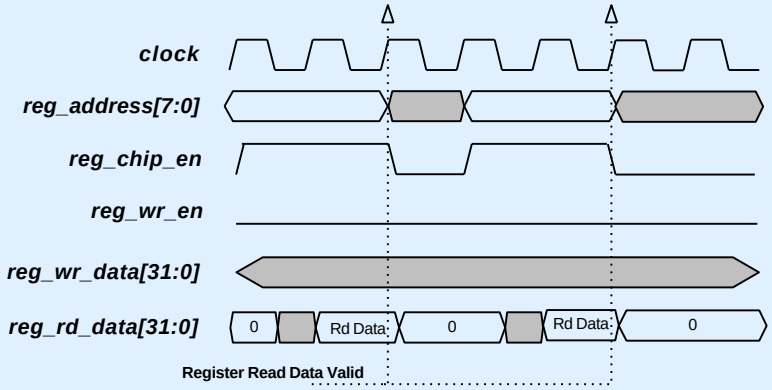
Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0006 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
ADC Interface	
ADC IF / I	IF data (or I data) sampled at CLOCK rate. Format configurable between 2's complement and offset binary.
ADC Q	Q data sampled at CLOCK rate (not used when IF sampling is used). Format configurable between 2's complement and offset binary.
AGC PWM Control	AGC pulse width modulated output for signal level control at the ADC input(s).
Constellation Outputs	
Symbol Valid	Active-high enable (CLOCK width) indicating that the constellation outputs should be sampled on the next CLOCK rising edge.
Symbol Data	De-mapped constellation output data.
Soft Data I	Demodulated constellation output.
Soft Data Q	
Sliced Data I	Demodulated and sliced constellation output.
Sliced Data Q	
Signal quality estimate	The input signal quality estimated from the constellation noise.
Demodulator locked	Active-high flag indicating that the demodulator has successfully acquired and demodulated the input constellation. Can be used to flag FEC start.
Others	
clock	Clock input – should be no less than 2·5 x the bandwidth occupied by the modulation.
reset_n	Asynchronous active-low reset input.

Register Interface

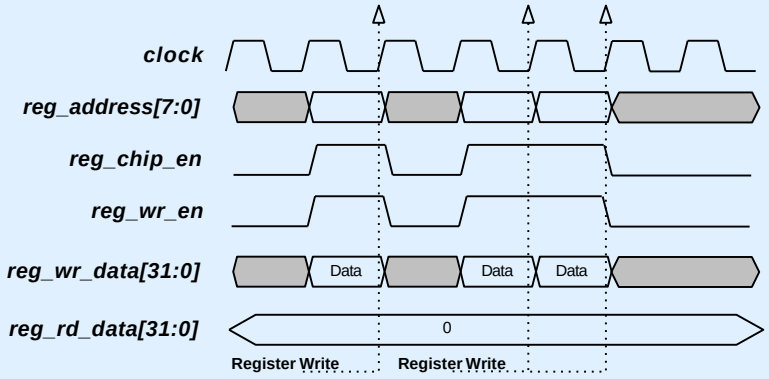
A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

An active-high interrupt line is also available.

Register read access:

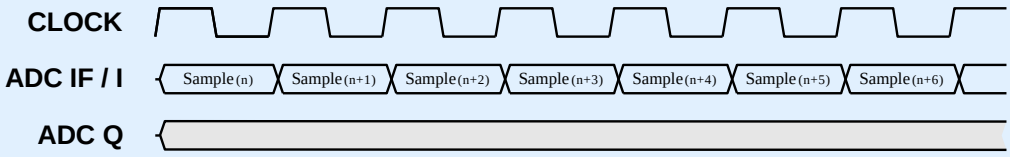


Register write access:

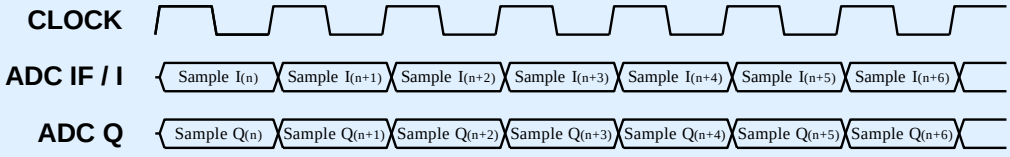


Timing Diagrams

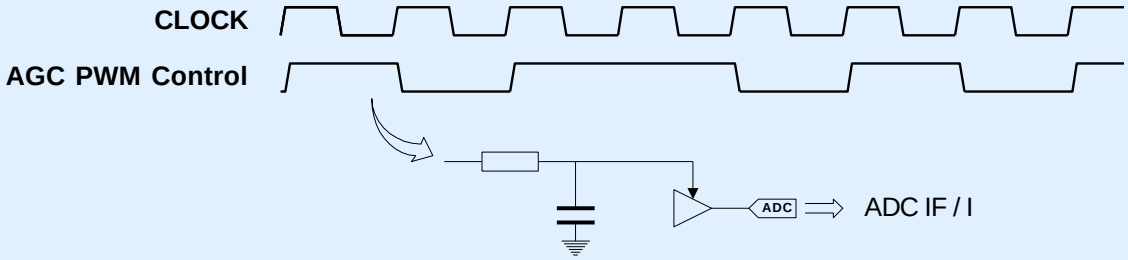
ADC IF Interface:



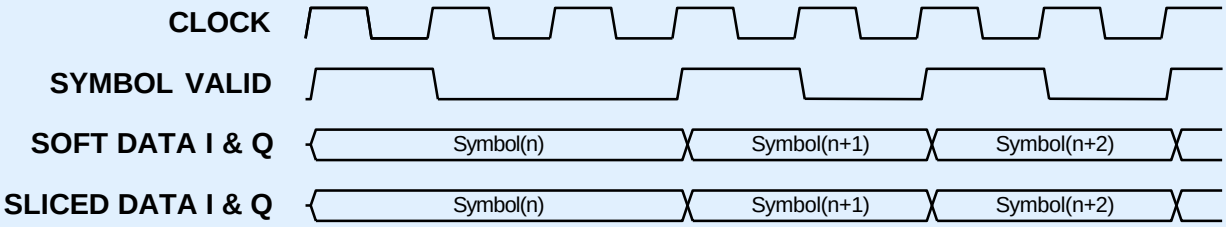
ADC I/Q Interface:



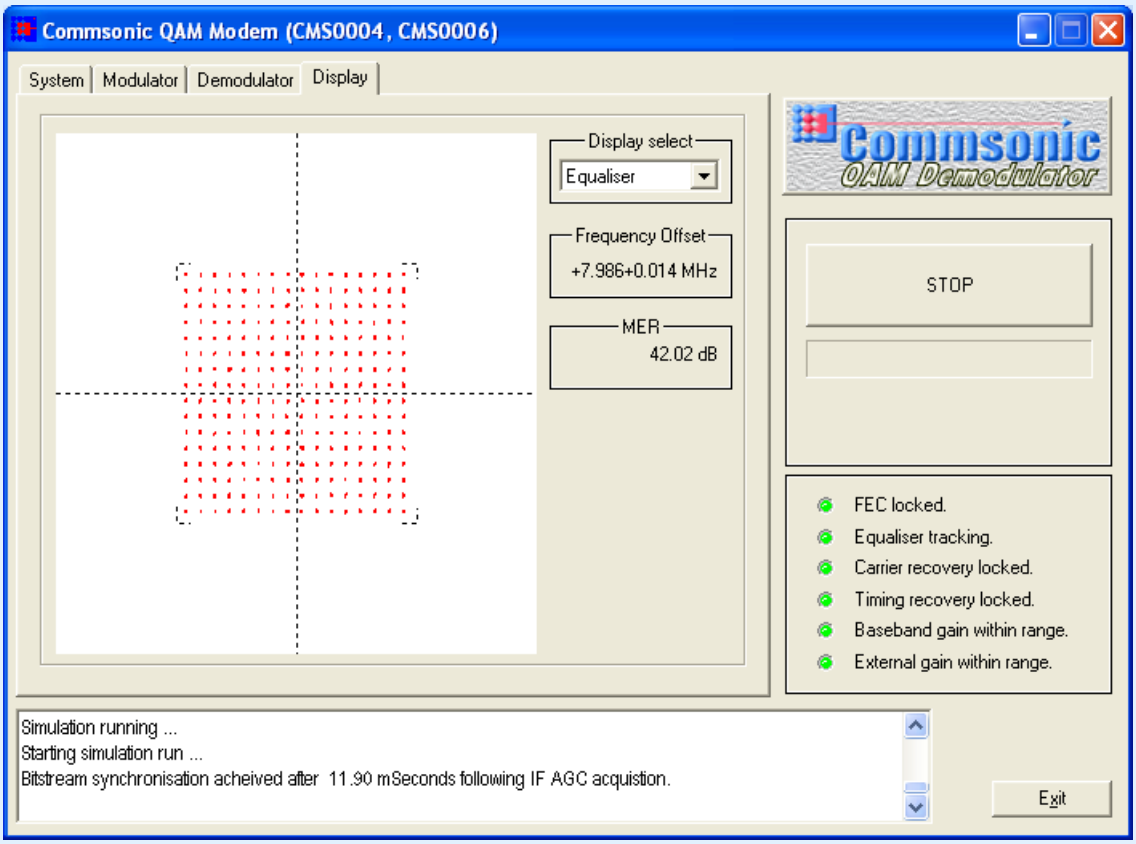
External Gain Control:



Constellation Output:



EVALUATION



EXAMPLE APPLICATIONS

Application	Configuration
Point-to-point terrestrial microwave (backhaul), 56MHz channel	32-QAM @ 40Ms/s provides sufficient capacity for an STM-1/SDH link allowing overhead for FEC.
Point-to-point terrestrial microwave (backhaul), 28MHz channel	128-QAM @ 24Ms/s provides sufficient capacity for an STM-1/SDH link allowing overhead for FEC.
Point-to-multipoint wireless MAN (IEEE 802.16-SC) 25MHz channel	64-QAM @ 20Ms/s provides 120Mb/s raw
Unlicensed 5GHz UNII band, 20MHz channel	128-QAM @ 17Ms/s to provide 100Mb/s post FEC.

About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/S2/DSNG, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2, ATSC and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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